



Cadence User Conference 2017

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Hierarchical circuit diagrams for layout and PSpice with Capture
16.05.2017

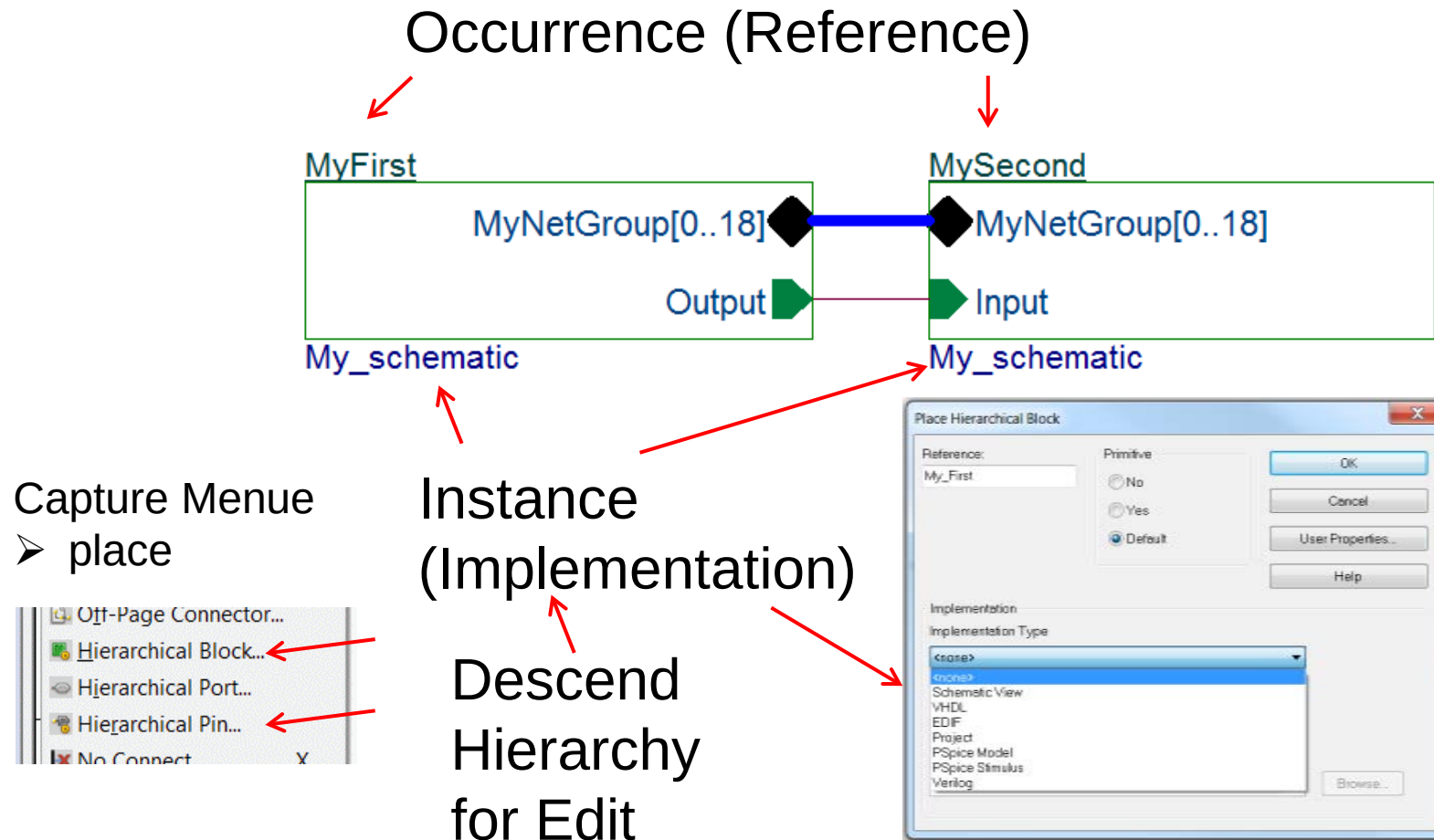
Motivation:

- Usually circuit diagrams are drawn with many A3 sized sheets on the same hierarchical level
- Very often a block diagram is drawn with a tool outside the schematic editor (PowerPoint, Visio)

Restrictions of these solutions:

- It is difficult to get an entry point of the project
- Multiple sheets are necessary for the work on a detail
- Modifications have to be done on several copied circuits
- Block- and circuit diagrams are not consistent
- Detailed knowledge of the implementation is necessary for modifications (PSpice)

Orcad Capture elements for hierarchical designs:



Top Down Method:

Place Block

Define Instance

Define Occurrence

Place Pins

Place Connections

Descend Hierarchy

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Capture elements for hierarchical designs:

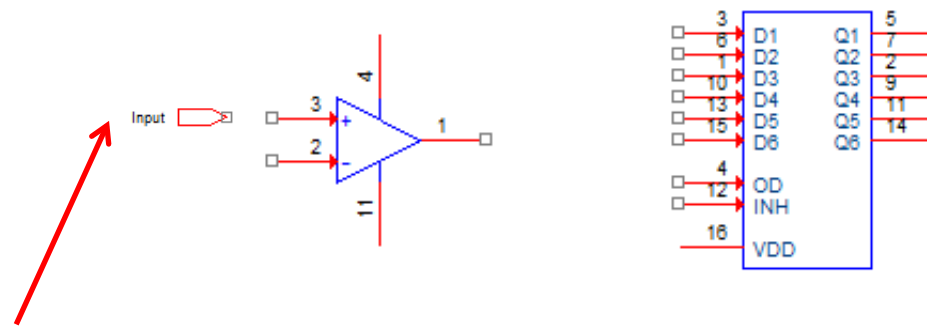
Bottom up Method (1):

Open flat design

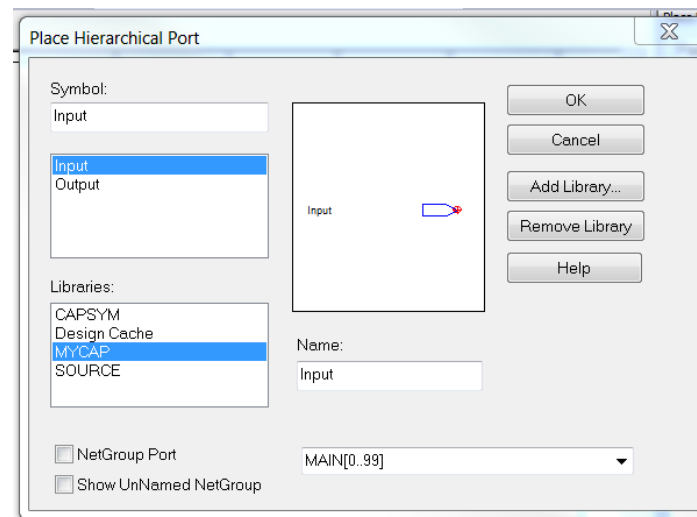
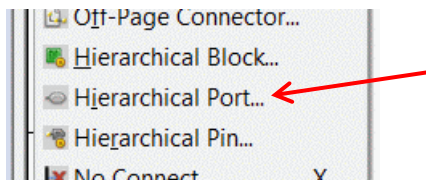
Place Ports

Select Symbol

Place Symbols(s)

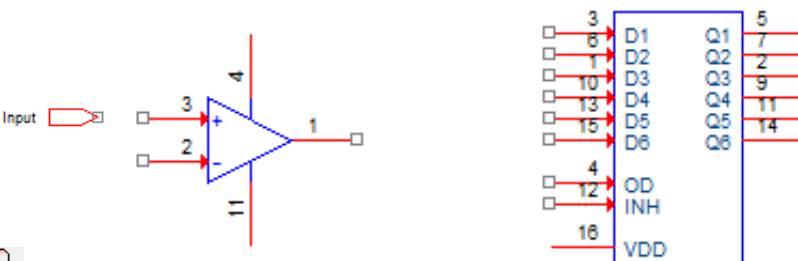


Capture Menue
➤ place



Capture elements for hierarchical designs:

Bottom up Method (2):



Input

Start Page MyBlk* ppt_elem.*

New Property... Apply Display... Delete Property

Input

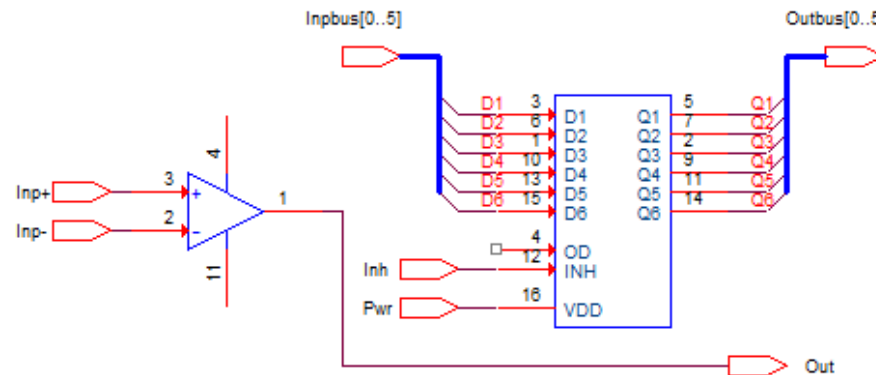
A	
Color	Default
Connected Net name	PORTRIGHT-R
Location X-Coordinate	220
Location Y-Coordinate	380
Name	PORTRIGHT-R
Source Library	C:\CADCENCE\SPB_17.2
Source Symbol	PORTRIGHT-R
Type	Input

Select Properties

- Input
- Bidirectional
- Output
- Open Collector
- Passive
- 3 State
- Open Emitter
- Power

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Capture elements for hierarchical designs:



Repeat and
Connect

Bottom up Method (3):

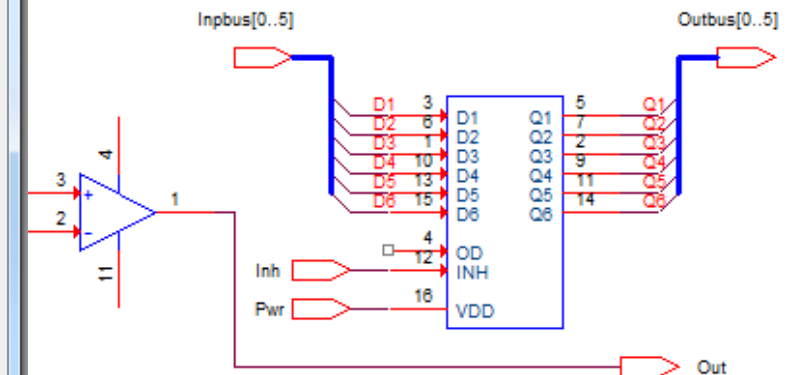
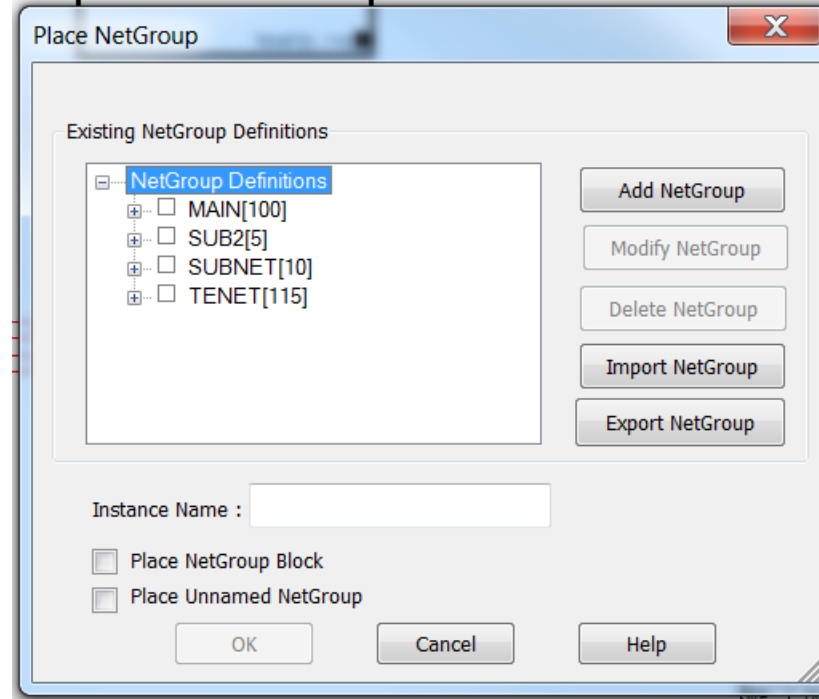
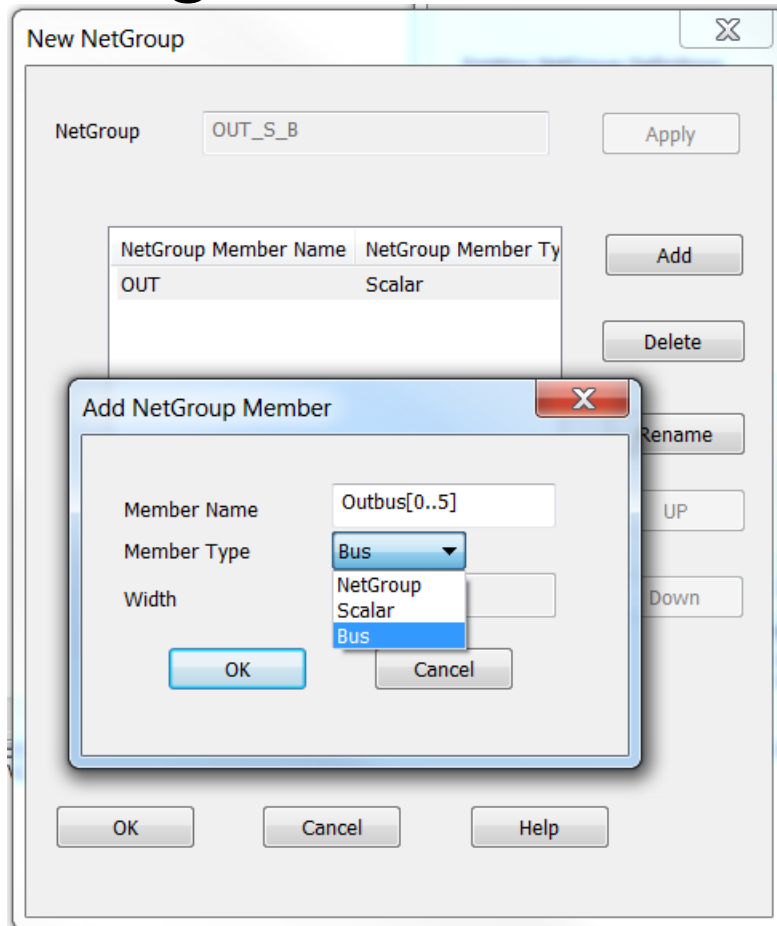
Place Ports
Select Symbol
Place Symbols(s)
Select Properties

Placement of the Hierarchical Blocks in
the upper levels like in Top Down Method

- Hierarchical Pins in the Block are generated
based on the Hierarchical Ports

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Single Lines, Busses and NetGroups (1):

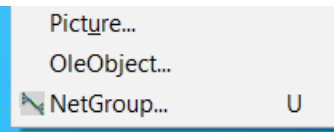


NetGroup Connection:

Open design

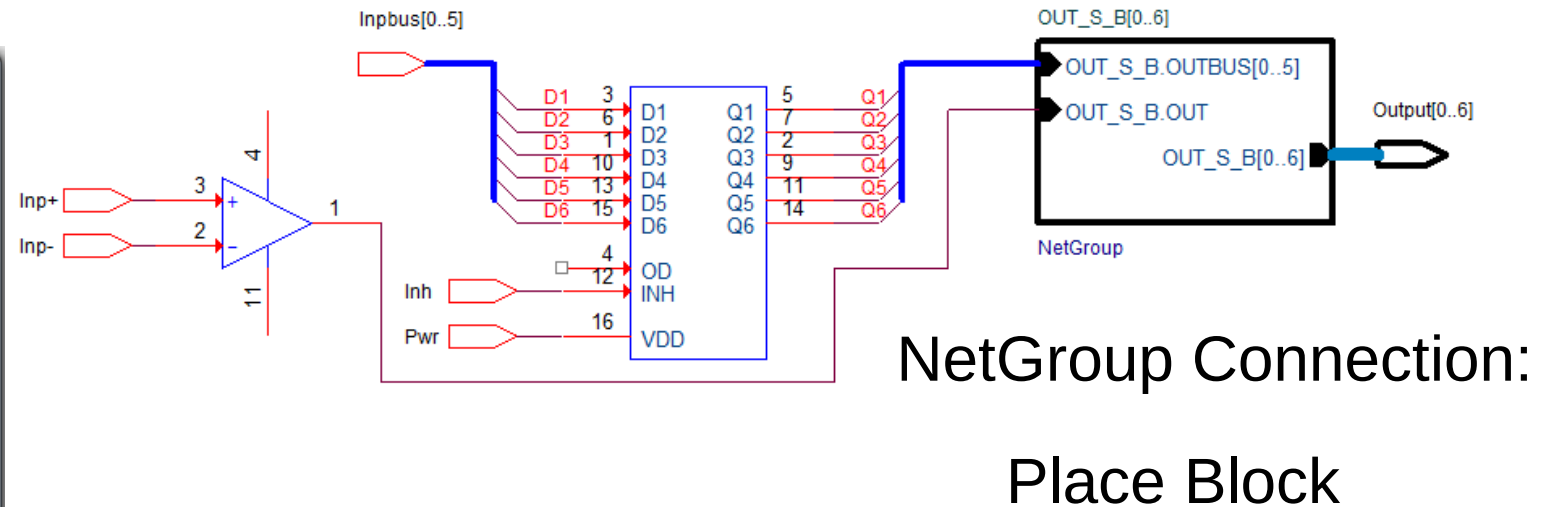
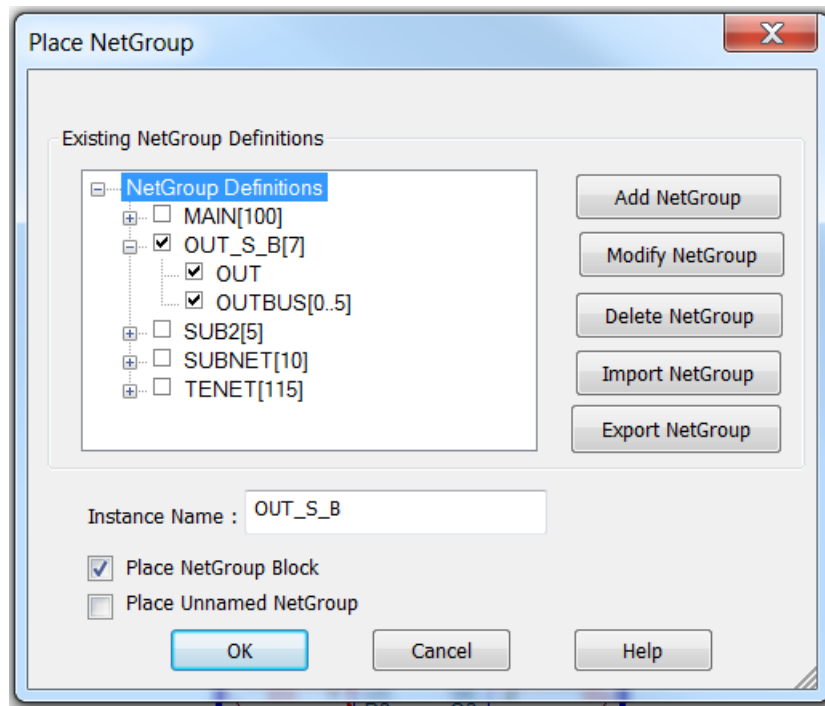
Define NetGroup

Capture Menu
➤ place

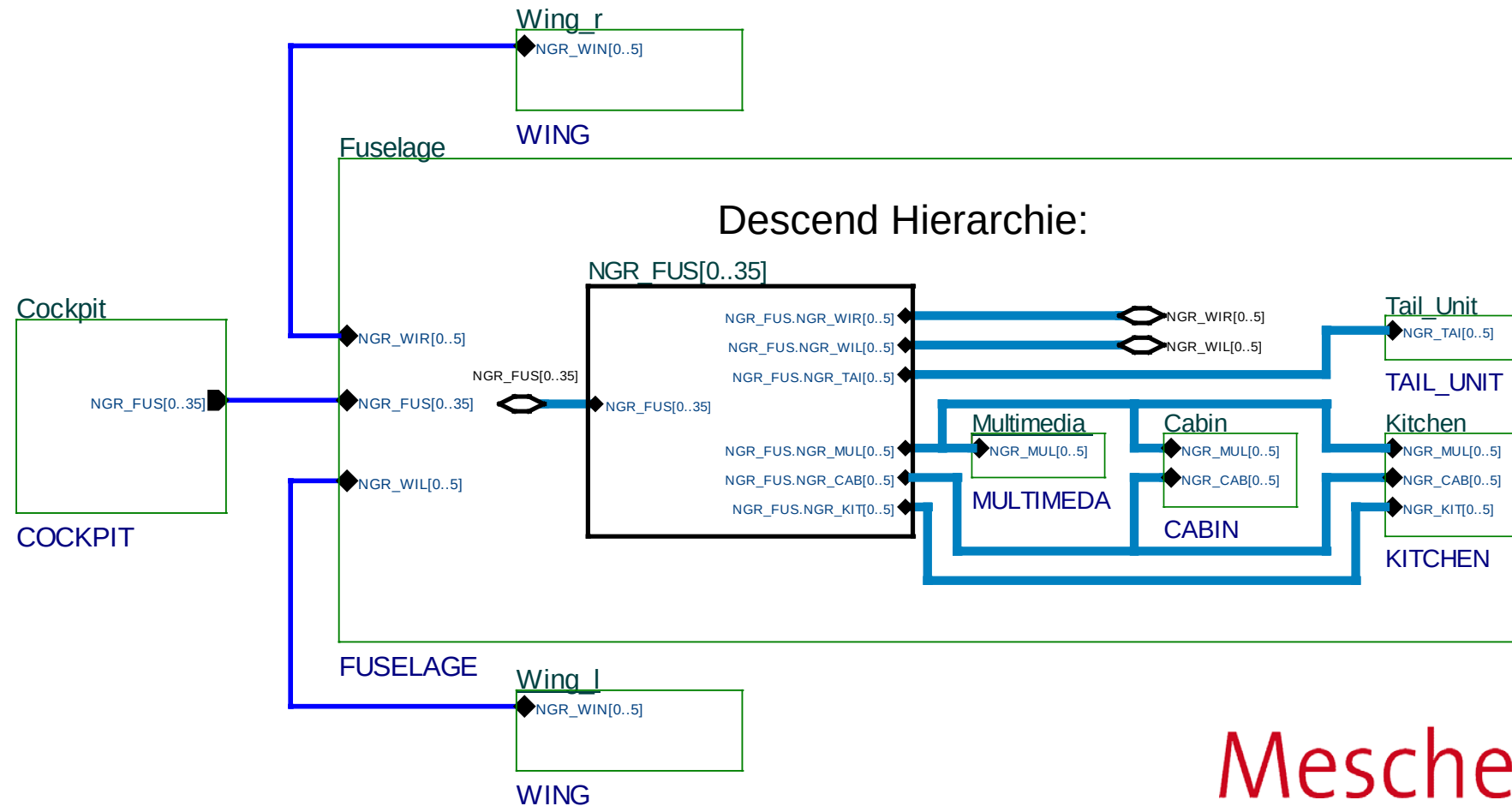


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Single Lines, Busses and NetGroups (2):



Main Page of a large Project (Airplane):



PSpice with local Parameters:

2nd_order_Bessel

$R_{fb} = 4.45k$

$f_g = 20MEG$

SUBPARAMETERS:

$R_{fb} = 3.85k$

$f_g = 20MEG$

PARAMETERS:

$R_{in} = 1k$

$v = \{ @R_{fb} / R_{in} \}$

$\omega_m = \{ 2 * \pi * @f_g \}$

PARAMETERS:

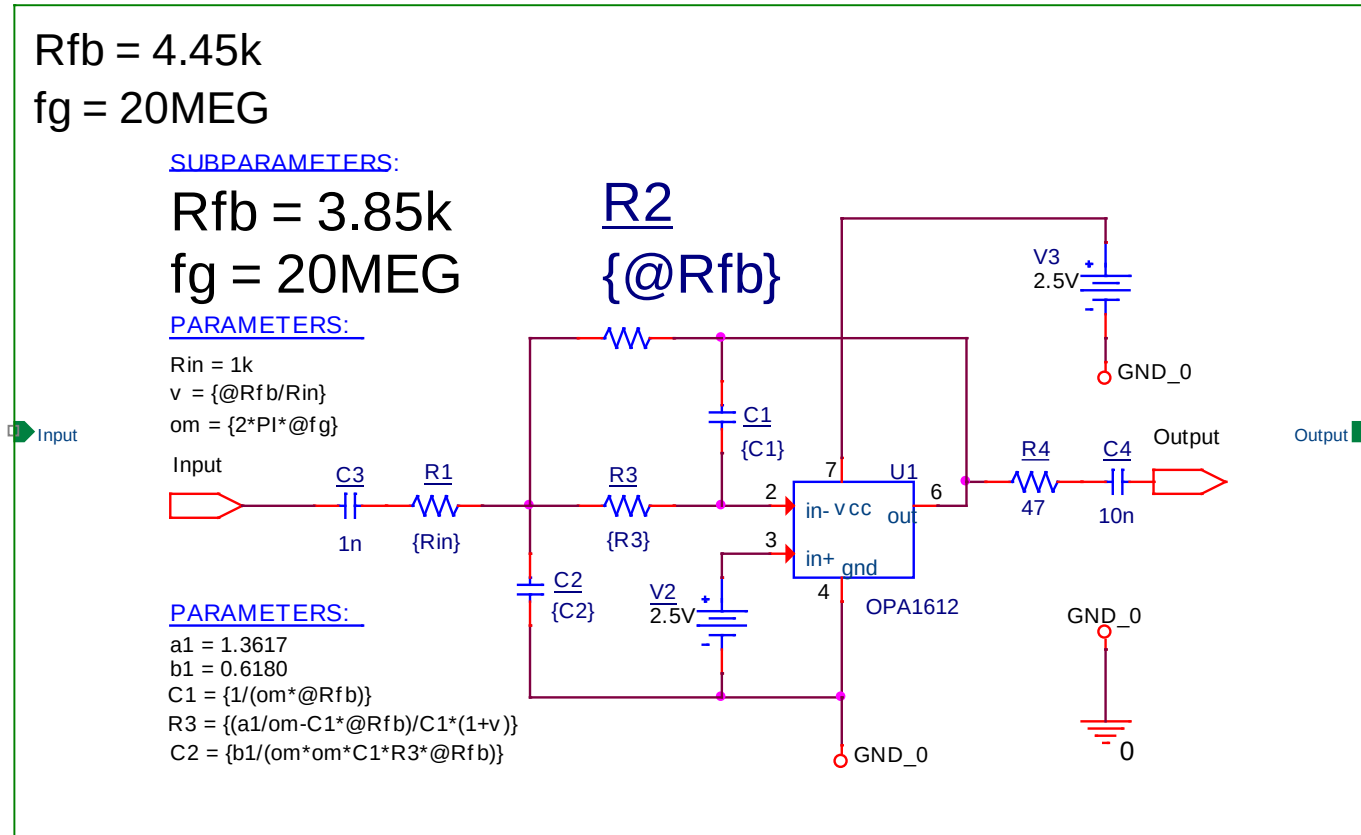
$a_1 = 1.3617$

$b_1 = 0.6180$

$C_1 = \{ 1 / (\omega_m * @R_{fb}) \}$

$R_3 = \{ (a_1 / \omega_m - C_1 * @R_{fb}) / C_1 * (1 + v) \}$

$C_2 = \{ b_1 / (\omega_m * \omega_m * C_1 * R_3 * @R_{fb}) \}$



OPAMP_D

Start Page	PBL	PCON	P
New Property...	Apply	Display...	Dr
			A
			PSPICE_BL : PBL : 2n
BiasValue Power	36.60mW		
Color	Default		
fg	20MEG		
Implementation	OPAMP_D		
Implementation Path			
Implementation Type	Schematic View		
Location X-Coordinate	100		
Location Y-Coordinate	50		
Name	OPA211_1		
Primitive	DEFAULT		
Reference	2nd_order_Bessel		
Rfb	4.45k		
Value	OPAMP_D		
Vdelta_ref	{Vdelta_tst}		

e.g.

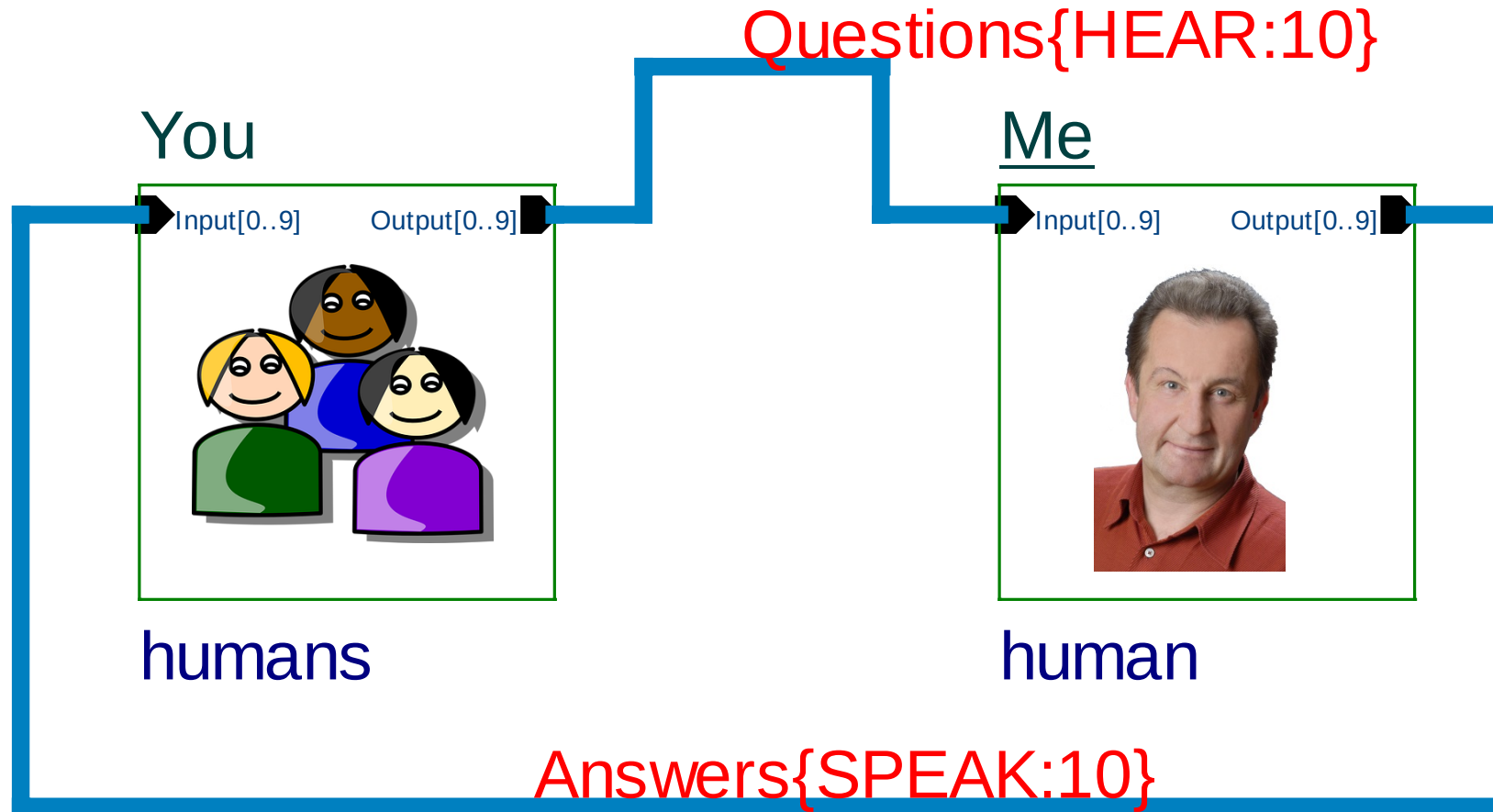
Halbleiter-Schaltungstechnik

U. Tietze Ch. Schenk

Springer Verlag

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